Please replace the paragraph beginning on page 9, line ~~6~~ 12 with the following amended paragraph: SB 2/9/07

For further description, the present invention is to provide a method of manufacturing a TFT-LCD array panel. The method can be applied in the pixel electrode circuit of a TFT-LCD array panel. Please referring to Figure 2, it presents the circuit layout of the pixel electrode. It comprises a transparent conducting electrode 23, a gate electrode 21, and a storage capacitor electrode 22. Also, they are formed on the substrate 10 in the first masking process. Then, using the selective sputtering method deposits the first metal wires 211, 221. Further, the contact window of the transparent conducting electrode is implemented in the in the second masking process. More, the depositions of the second metal wires 63, 64, 65 are implemented in the third masking process. Finally, the deposition of the passivation layer 70 is implemented for forming a pixel electrode.

AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning on page ~~8~~ 7, line ~~24~~ 3 with the following amended paragraph: SS 2/9/07

Accordingly, please referring to Figure 1b, a dielectric layer, an A-Si layer and a poly-Si layer are deposited as shown in the figure. Further, a dielectric layer 30, and an A-Si layer 40 and a poly-Si layer 50 are deposited in order, and are covered on the substrate 10, the gate electrode 21, the storage capacitor electrode 22 and the transparent conducting layer 23. Then, performing the second masking process. Please referring to Figure 1c, it is one of the preferred embodiments according to the present invention showing the contact window in the masking process. Firstly, photo-resists 501, and 502 are used to shield the outside of the transparent conducting electrode 23. Then, the contact window 24 is defined in the masking process. Please referring to Figure 1d, it is one of the preferred embodiments according to the present invention showing the contact window formed in the etching process. Then, the photo-resists 501, 502 are removed. More, the deposition method forming an A-Si layer, a transparent conducting electrode, or a gate electrode can use PVD, low pressure CVD, or plasma enhanced CVD to implement.

Please replace the paragraph beginning on page 8, line ~~8~~ 14 with the following amended paragraph: SS 2/9/07

Further, it presents a photo-resist lift-off process. Please referring to Figure 1g, it is one of the preferred embodiments according to the present invention showing a photo-resist lift-off process for implementing the deposition of the second metal wiring. Then, it uses the poly-Si layer ~~51~~ 50 with etching technique to block the channel of the source and drain electrodes thereto the operational channel 411. Please referring to Figure 1h, it is one of the preferred embodiments showing the operational channel according to the present invention. The second metal wire can be made of the low-resistance metal materials, such as Al, Cu, Ag, Mo, Cr, Ti, W, or the induced material such as diffusion, and adhesion with multi-layer structure of the metal material.